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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,404	12/06/2001	Koji Nii	027260-505	5384

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EXAMINER	
TRAN, TAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,404	NII ET AL.	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 10/15/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-15* is/are rejected.

7)☒ Claim(s) *10-12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The indicated allowability of claim 5 is withdrawn in view of the newly discovered reference(s) to claim 5. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 8, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al. (6,190,953) (of record) in view of Igarashi et al. (6,299,314) (of record).

With regard to claims 1,4, Igarashi et al. (6,190,953) discloses a gate electrode 4 formed on a substrate 1 through a gate insulating film 3 lying therebetween; first and second diffused layers (2A,2B) formed opposite to each other across the portion of the substrate 1 existing under the gate electrode 4 and having a first conduction type, each having a second conduction type different from the first conduction type of the portion; a wiring layer 11 above the gate electrode 4; and a contact 18 formed within a contact hole between the wiring layer 11 and the substrate 1; the first diffused layer 21A electrically connecting the wiring layer 11 to the contact 18 and contact electrically connecting to the sidewall of the gate electrode 4, and a third diffusion layer 2C that connects the first and second layers (2A,2B). Note figs. 4C-4E and 6B,7F of Igarashi et al. (6,190,953) and see attachment #1.

Igarashi et al. (6,190,953) does not disclose contact hole having a width which spans the gate electrode and the first diffused layer.

However, Igarashi et al. (6,299,314) discloses contact hole CH14 having a width which spans the gate electrode 3 and the first diffused layer 7A. (Note fig. 22 of Igarashi et al. (6,299,314), and see attachment #2).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Igarashi et al. (6,190,953)'s device having contact hole having a width which spans the gate electrode and the first diffused layer such as taught by Igarashi et al. (6,299,314) in order to prevent the short-circuit between the gate electrode and wiring layer.

With regard to claim 2, Igarashi et al. (6,190,953) discloses the contact 18 is connected also to the second diffused layer 2B. Note fig. 7F of Igarashi et al. (6,190,953).

With regard to claim 3, Igarashi et al. (6,190,953) discloses a third diffused layer 2C formed on the substrate 1; and an isolation area 20 formed between the first and the third diffused layers (2A,2C), which separates the first and the third diffused layers (2A,2C) each other; wherein the contact 18 is connected further to the third diffused layer 2C. Note fig. 7F of Igarashi et al. (6,190,953).

With regard to claim 5, Igarashi et al. (6,299,314) discloses the contact CH14 is connected the first and second diffused layers 7. Note fig. 22 of Igarashi et al. (6,299,314)).

With regard to claim 6, Igarashi et al. (6,190,953) discloses another diffused layer 2D formed on the substrate 1; and an isolation area 20 formed between the first portion of the diffused layer 2A and the another diffused layer 2D, which separates the first portion of the

diffused layer 2A and the another diffused layer 2D, wherein the contact is connected further to the another diffused layer 2D. Note fig. 7F of Igarashi et al. (6,190,953).

With regard to claims 7, 8, 13, 14, Igarashi et al. (6,190,953) and Igarashi et al. (6,299,314) do not disclose the gate 4 is a memory node of the SRAM cell or the memory node of a bistable trigger circuit. However, it would have been obvious to one of ordinary skill in the art to form the gate 4 of Igarashi et al. functions as a memory node, because it is conventional in the art to use one of the gate electrodes that functions as a memory node. Note Fig. 1 of Sunami is cited to support for the well known position. Although Igarashi et al. does not teach exact the type of the device as that claimed by Applicant, the type differences are considered obvious design choices and are not patentable unless unobvious or expected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note in re Leshin, 125 USPQ 416.

Claims 9,15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al. (6,190,953) in view of Igarashi et al. (6,299,314) and further in view of Yaegashi et al. (6,472,701)) (of record).

With regard to claims 9,15, Igarashi et al. disclose another gate electrode 4 formed on the substrate 1 through another gate insulating film 3, and a transistor for composing a semiconductor integrated circuit therein.

Igarashi et al. (6,190,953) and Igarashi et al. (6,299,314) do not disclose the film thickness of the gate insulating film is thinner than the one of the another insulating film.

However, Yaegashi et al. discloses the film thickness of the gate insulating film 105 is thinner than the one of the another insulating film 108. (Note fig. 1 of Yaegashi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Igarashi et al. (6,190,953) and Igarashi et al. (6,299,314)'s device having the film thickness of the gate insulating film is thinner than the one of the another insulating film such as taught by Yaegashi et al. in order to elevate the speed of a peripheral transistor outside the memory.

Allowable Subject Matter

3. Claims 10-12, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-12, 16 allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as the relative dielectric constant of the gate insulating film is higher than the one of the another gate insulating film as recited in claims 10,16, the impurity concentrations of the first diffused layer and the second diffused layer are higher than the ones of the source and the drain areas as recited in claim 11, the impurity concentrations of the diffused layer are higher than the impurity concentration of the source area and the drain area as recited in claim 12.

Response to Amendment

4. Applicant's arguments with respect to claims 1-9,13-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Nov 2003

Minhloan Tran
Primary Examiner
Art Unit 2826